**Ex No:6**

**Date: 18.10.2024**

**STUDY OF XILINX TOOL WITH FPGA TRAINER KIT**

**Aim:**

To study Xilinx Software with FPGA Trainer kit by implementing a Full Adder.

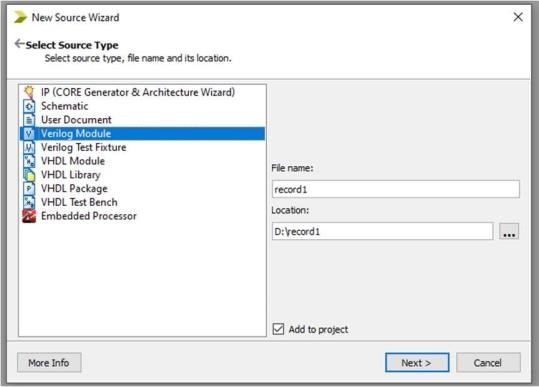
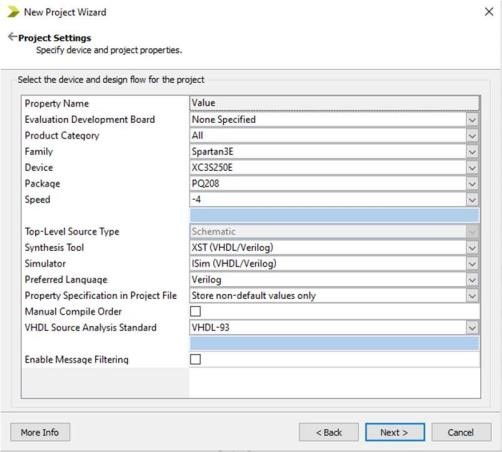
**SOFTWARE AND APPARATUS REQUIRED:**

Xilinx ISE Design suite 13.1 version software and FPGA Trainer kit.

**PROCEDURE:**

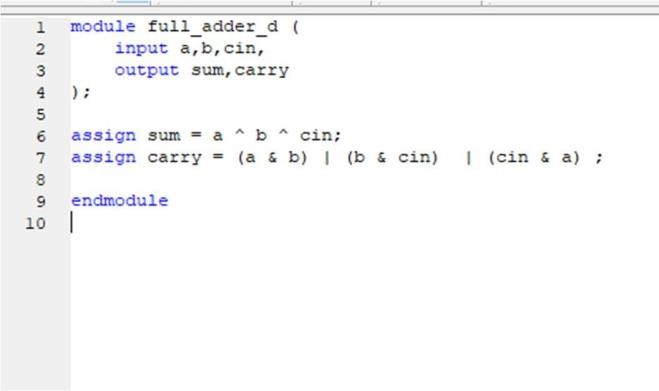
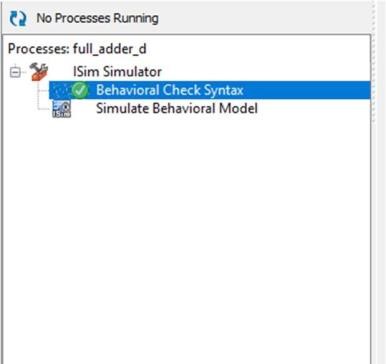
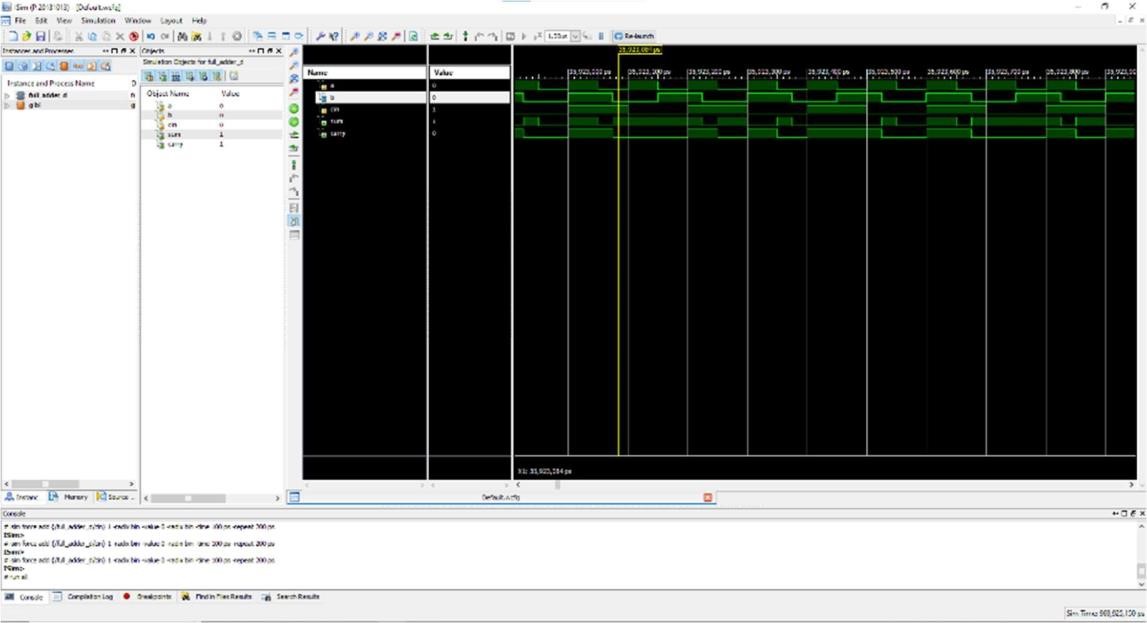
Steps to compile Verilog HDL code:

* Open Xilinx ISE Design Suite 13.1 Version Tool.
* Go to ‘file’ option, select ‘New Project’ and open it.
* Name the project file at location D or location E, select the top-level source as schematic, click ‘Next’.
* Set the values in the project settings window.
* Right click on the project name and click new source.
* Enter the project name as the file name and select the Verilog module



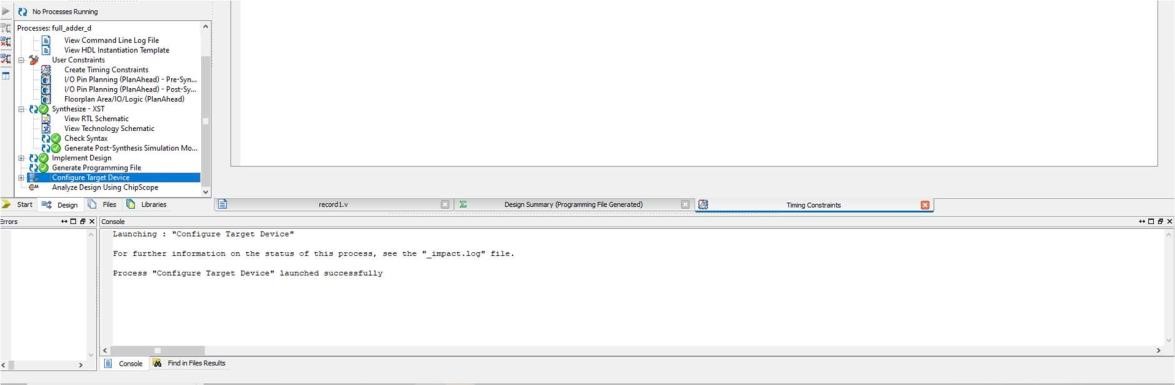
**Steps for simulation:**

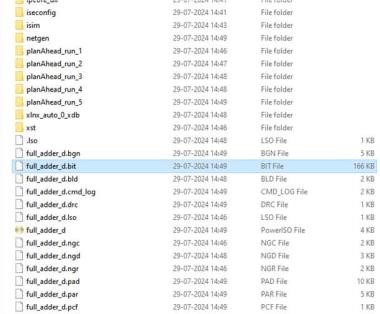
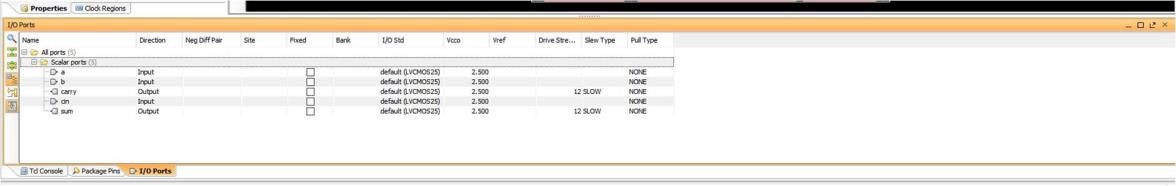
* In the view panel, click simulation and click the source name.
* In the process, under ISIM Simulator
  + Click on Check the behavioral syntax
  + Click on the Simulate Behavioral Model
* Force clock all the input values in the ISIM window.
* Click the run button and verify the output



**Steps to implement in FPGA Trainer kit:**

* In the view panel, click the implementation button.
* Under Process, check design Summary/reports.
* Under Design Utilities, Run all the process.
* Under User constraints, Run timing constraints and Pre-Synthesis on Plan Ahead
* Software. In Plan Ahead, set the Pins in the site column.
* Run the Post synthesis and Floor Plan Area I/O logic.
* Under Synthesize and Implement Design, Run all the process
* Generate the Programming File.
* In the project location, copy the BIT file and paste it in FPGA Download folder and
* name it as output.bit.
* Execute the prog file in the FPGA Downloader folder and click the prog button on the
* kit. Change the inputs in the kit and verify the Outputs.





A computer screen with white text

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**EXAMPLE:**

**Full adder:**

**Logic Diagram:**

A diagram of a computer code

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**Truth Table:**

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**Verilog code for full adder:**

//full adder using data-flow modeling

module full\_adder (

input a,b,cin,

output sum,carry

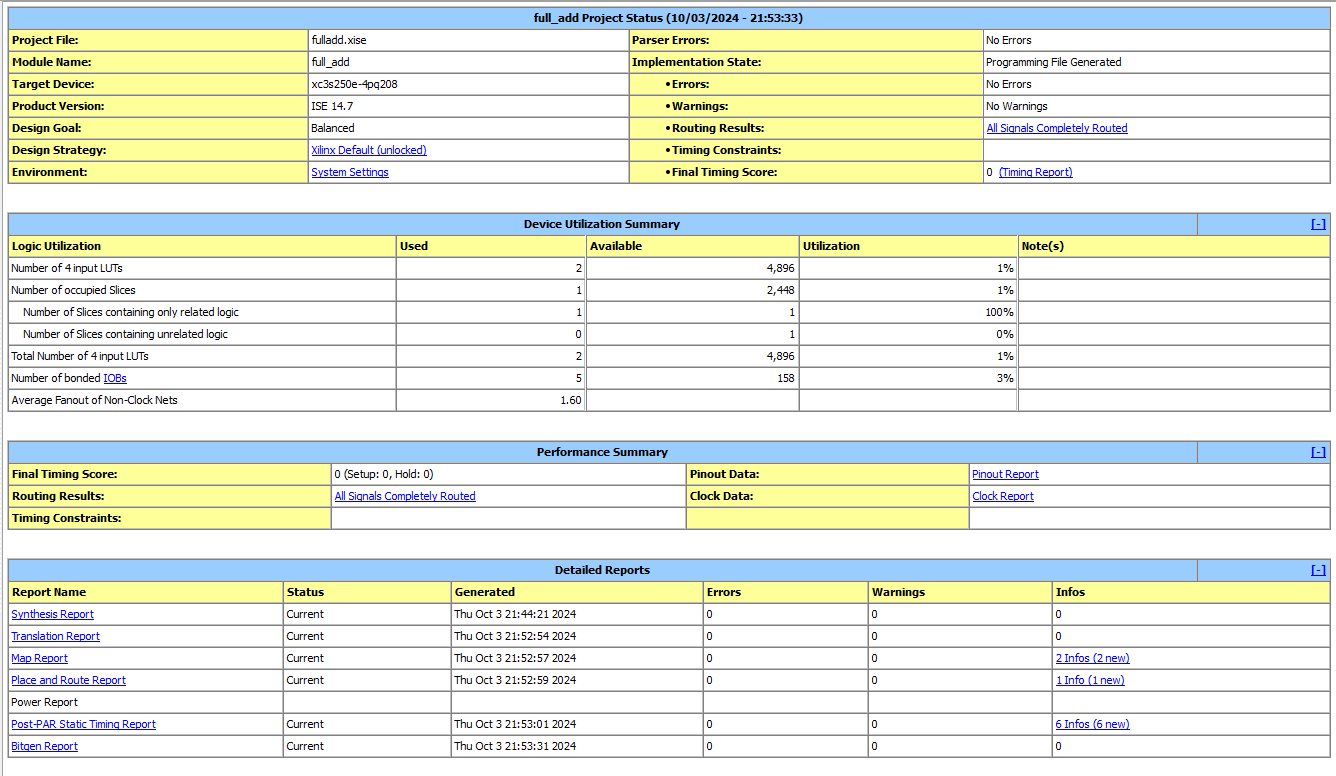
);

assign sum = a ^ b ^ cin;

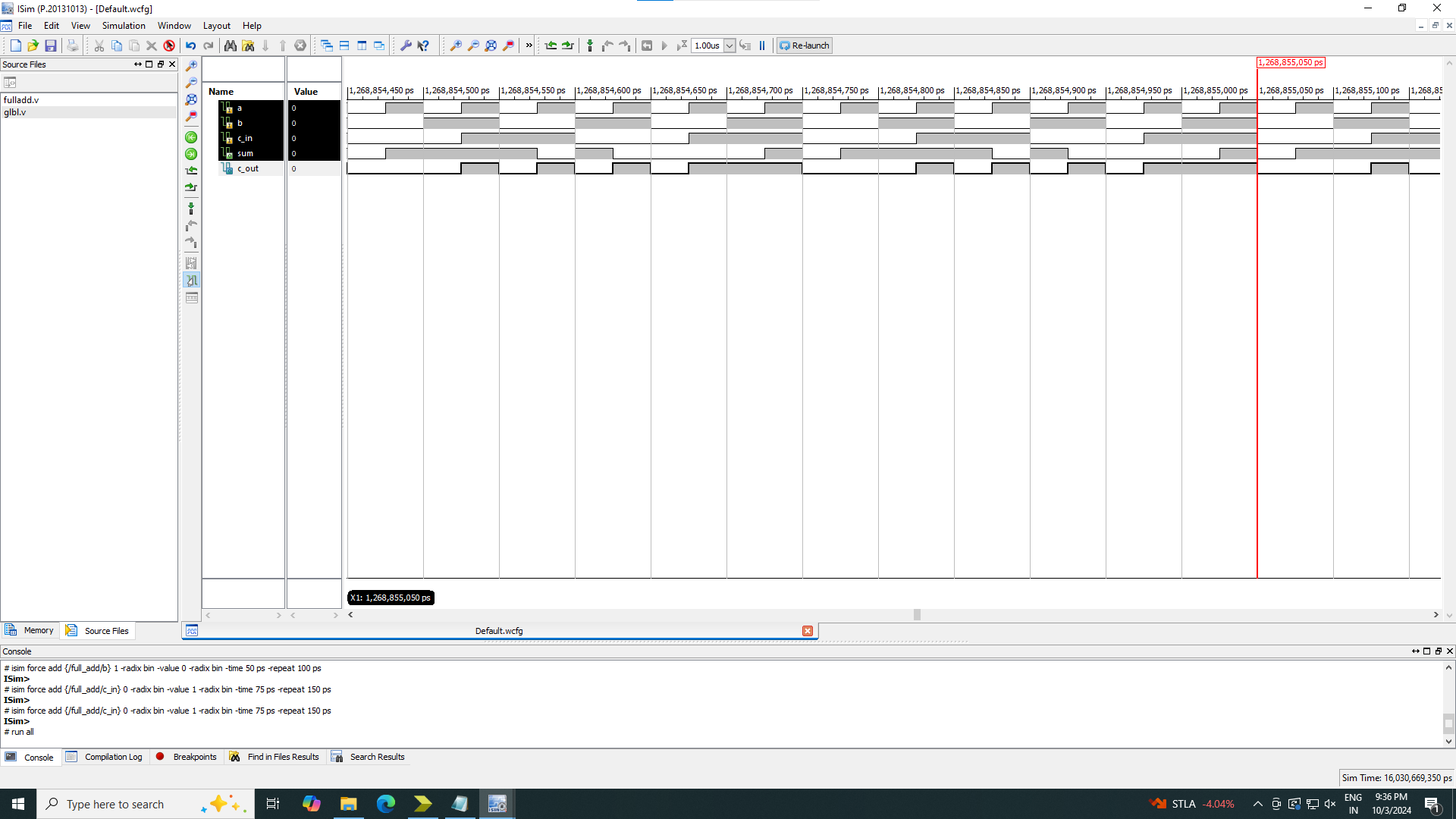
assign carry = (a & b) | (b & cin) | (cin & a) ;

endmodule

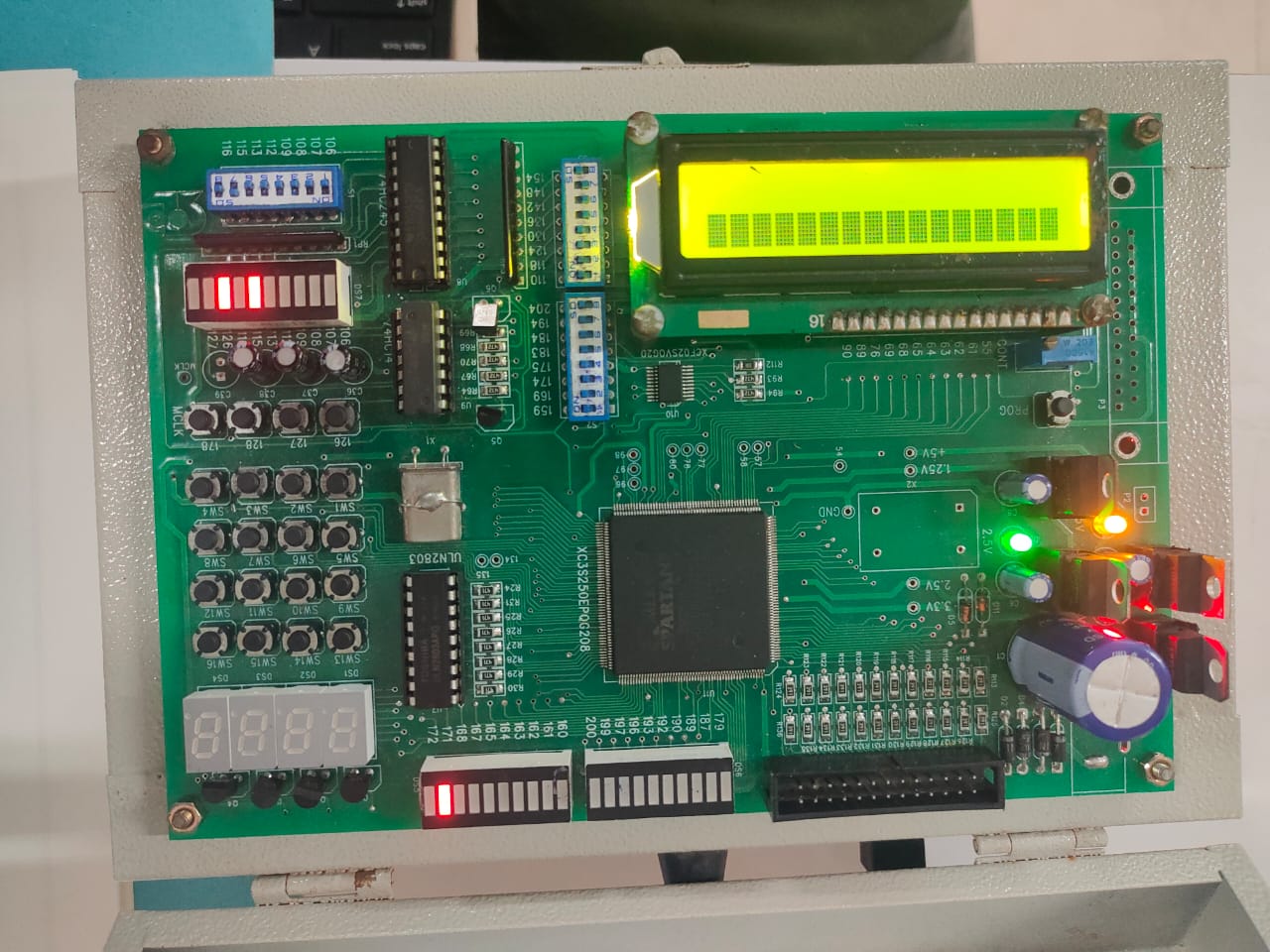
**Synthesis report:**

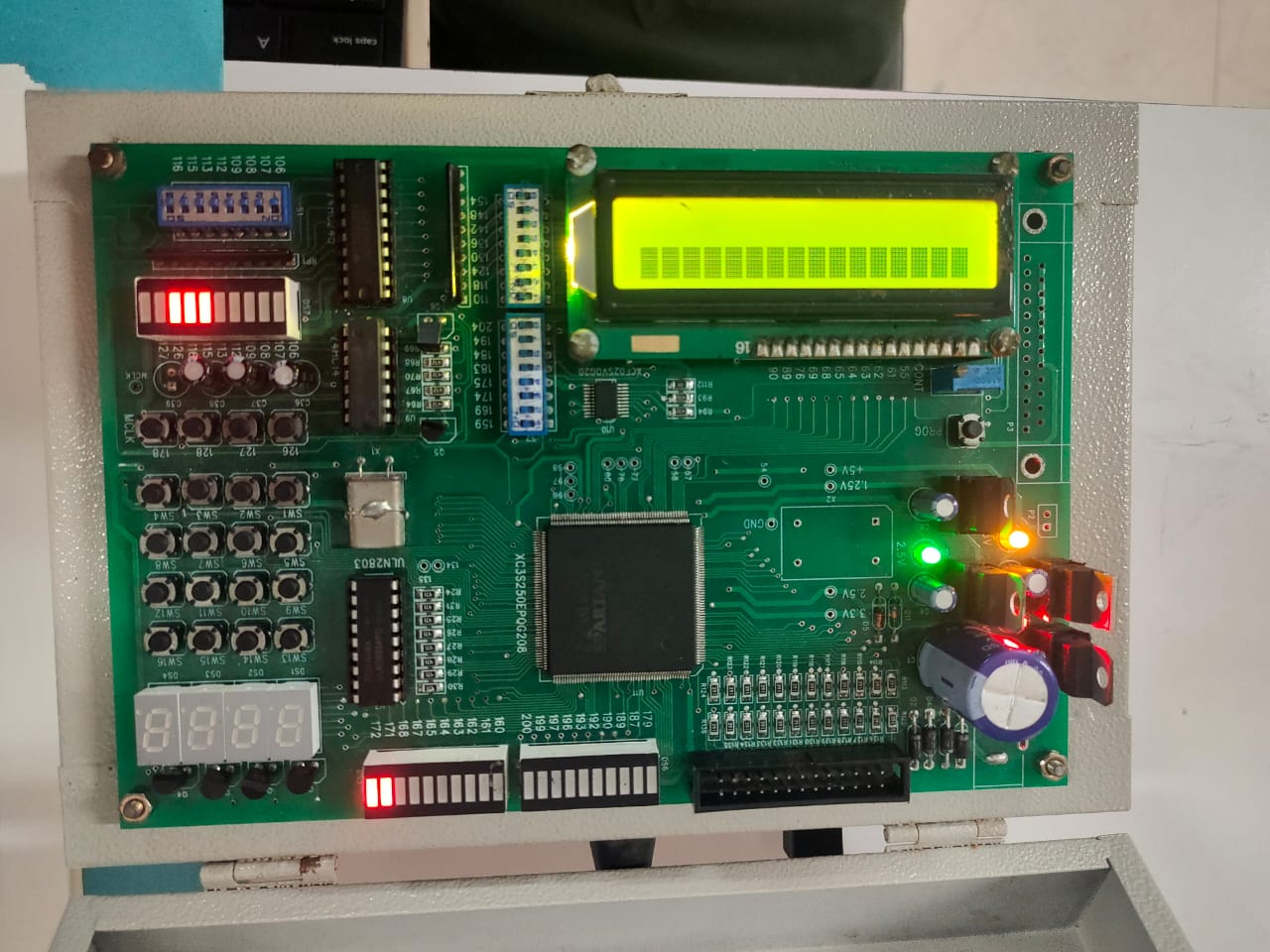


**Simulated Output:**



**FPGA Trainer Kit Photos:**





**Result:**

Thus, the Xilinx tool and FPGA Trainer kit is studied by implementing a full adder and the output is verified successfully.